BS Computer Engineering Long Term Assessment Plan

PROGRAM LEARNING OUTCOMES (PLOS)

1. An ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics**. (ILO 1)**
2. An ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors. **(ILO 1 & 5)**
3. An ability to communicate effectively with a range of audiences. **(ILO 2)**
4. An ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts. **(ILO 3, 4 & 5)**
5. An ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives. **(ILO 3 & 4)**
6. An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions. **(ILO 1 & 2)**
7. An ability to acquire and apply new knowledge as needed, using appropriate learning strategies. **(ILO 1, 2, & 4)**

Assessment Plan:

Year 1: 2021-2022	
1. *Which PLO(s) to assess*	2. An ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors. **(ILO 1 & 5)**
2. *Assessment activity*	Exam Problems
3. *Assessment instrument*	Program rubric
4. *Sample (courses/# of students)*	ENGR 330 Electric Circuits
5. *SLO from the course*	1) Analyze and compute voltage, current, and power in circuits with passive and active components. 2) Understand the design and operation of transistor amplifiers. 3) Understand small- and large-signal models and DC operating points for circuit components. 4) Understand the design and operation of digital circuit components. 5) Utilize circuit analysis software and hardware to compute electrical quantities in transistor-based circuits. 6) Develop greater general knowledge of household electronic devices
6. *Time (which semester(s))*	Spring 2019

7. *Responsible person(s)*	Prof. Doering
8. *Ways of reporting (how, to who)*	The results (quantitative and qualitative) will be reported by faculty to the department chair via completion of the course Faculty Self-Assessment form.
9. *Ways of closing the loop*	Interaction between chair, faculty and industrial advisory board

Year 2: 2022-2023	
1. *Which PLO(s) to assess*	6. An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions. **(ILO 1 & 2)**
2. *Assessment activity*	Final Project report and presentation
3. *Assessment instrument*	Program rubric
4. *Sample (courses/# of students)*	a-CMPE 344 Microprocessor Laboratory
5. *Time (which semester(s))*	a-Spring 2020
6. *Responsible person(s)*	a. Prof. Sumarsono
7. *Ways of reporting (how, to who)*	The results (quantitative and qualitative) will be reported by faculty to the department chair via completion of the course Faculty Self-Assessment form.
8. *Ways of closing the loop*	Interaction between chair, faculty and industrial advisory board

Year 3: 2023-2024	
1. *Which PLO(s) to assess*	4. An ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts. **(ILO 3, 4 & 5)**
2.Assessment activity	e-Final exam
3.Assessment instrument	Program rubric
4.Sample (courses/# of students)	e-CMPE 493 Senior Capstone: Senior Design II
5.SLO from the course	Apply science
6.Time (which semester(s))	e-Spring 2022;

7.Responsible person(s)	e-Prof. Tandon
8.Ways of reporting (how, to who)	The results will be reported by faculty to the department chair via completion of the course Faculty Self-Assessment form.
9.Ways of closing the loop	Interaction between chair, faculty and industrial advisory board

Year 4: 2024-2025	
1. Which PLO(s) to assess	5. An ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives. (ILO 3 & 4).
2.Assessment activity	Senior design report and presentation
3.Assessment instrument	c-Capstone project rubric
4.Sample (courses/# of students)	c-CMPE 492, Senior Project I
5.SLO from the course	Successfully design a major capstone design project satisfying requirements of project clients. Disseminate project results through a technical journal article, mock U.S. patent application, and oral presentation in front of project clients. Experience working with project clients and team members. Understanding of the broad societal and ethical impacts of a project. Develop teamwork skills for project implementation and completion.
6.Time (which semester(s))	c-Spring 2023
7.Responsible person(s)	c-Prof. Tandon
8.Ways of reporting (how, to who)	The results (qualitative and quantitative) will be reported by faculty to the department chair via completion of the course Faculty Self-Assessment form.
9.Ways of closing the loop	Interaction between chair, faculty and industrial advisory board

Year 5: 2025-2026	
1. Which PLO(s) to assess	3. An ability to communicate effectively with a range of audiences. **(ILO 2)**
2. Assessment acivity	Senior design report and presentation
3. Assessment instrument	c-Capstone project rubric
4. Sample (courses/# of students)	c-CMPE 480, VLSI Circuit Design/Layout

5. *SLO from the course*	Understand NMOS and PMOS transistor operation and layout. Understand properties of silicon, polysilicon, metal, n-type and p-type materials for transistor layout designs. Create layouts of simple logic gates, combinational circuits, sequential circuit elements, and major CPU architecture components. Understand timing and delay properties digital circuit components, with respect to transistor sizing and layout. Understand design rules for transistor layout.
6. *Time (which semester(s))*	c-Spring 2024
7. *Responsible person(s)*	c-Prof. Tandon
8. *Ways of reporting (how, to who)*	The results (quantitative and qualitative) will be reported by faculty to the department chair via completion of the course Faculty Self-Assessment form.
9. *Ways of closing the loop*	Interaction between chair, faculty and industrial advisory board